JSD500P20A

Single P-Ch 200V Fast Switching MOSFETs

BVDSS		-200	V
ID@VGS=-10V , TC=25℃		-12	A
RDSON(MAX)	VGS = -10 V , ID = -5 A	780	mΩ

Features

- Super Low Gate Charge
- 100% EAS Guaranteed
- 100% DVDS tested
- Low Thermal resistance
- Low $R_{DS(ON)}$ to minimize conductive loss
- Advanced high cell density Trench technology

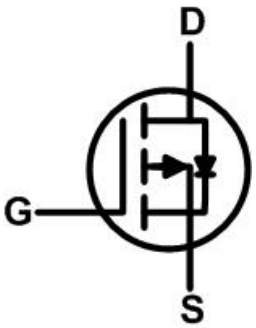
Application

- MB/VGA Vcore
- SMPS 2nd Synchronous Rectifier
- POL application
- BLDC Motor driver

Description

The EHD500P20A is the high cell density trenched P-Ch MOSFETs, which provide excellent RDSON and gate charge for applications.

The EHD500P20A meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Equivalent Circuit	Outline
	**TO-252** 

Package Marking and Ordering Information

Device Marking	Date Code	Device Package	Quantity
D500P20A	YWWXXX	TO-252	2500 pcs

Thermal Characteristic

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient [1]	50	℃/W
$R_{\theta JC}$	Thermal Resistance Junction-Case [1]	3.6	℃/W

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{DS}	Drain-Source Voltage	-200	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Continuous Drain Current, V_{GS} @ -10V [1] (T_C=25℃)	-12	A
	Continuous Drain Current, V_{GS} @ -10V [1] (T_C=100℃)	-7	
I_{DM}	Pulsed Drain Current [2]	-48	A
P_D	Total Power Dissipation [4] (T_C=25℃)	35	W
	Total Power Dissipation [4] (T_C=100℃)	14	
E_{AS}	Single Pulse Avalanche Energy [3]	36	mJ
I_{AS}	Avalanche Current	-12	A
T_J,T_{STG}	Operating Junction and Storage Temperature Range	-55 To 150	℃

Electrical Characteristics (T_J=25℃ unless otherwise noted)

Staic Characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V , I_D = -250 μA	-200			V
$R_{DS(ON)}$	Drain-Source On-State Resistance [2]	V_{GS} = -10 V , I_D = -5 A		500	780	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS} , I_D = -250 μA	-2.0		-4.0	V
I_{DSS}	Drain-Source Leakage Current (T_J=25℃)	V_{DS} = -200 V , V_{GS} = 0V			-1	μA
I_{GSS}	Gate-Body Leakage Current	V_{GS} = ±20 V , V_{DS} = 0V			±100	nA
gfs	Forward Transconductance	V_{DS} = -5 V , I_D = -3 A		9		S

Dynamic Characteristics						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
C_{iss}	Input Capacitance	V_{DS} = -160 V V_{GS} = 0 V f=1.0MHz		1210		pF
C_{oss}	Output Capacitance			170		pF
C_{rss}	Reverse Transfer Capacitance			45		pF
Switching Times						
Symbol	**Parameter**	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -160 V V_{GS} = -10 V R_G = 10 Ω I_D = -5 A		13.5		nS
t_r	Turn-On Rise Time			16		nS
$t_{d(off)}$	Turn-Off Delay Time			52		nS
t_f	Turn-Off Fall Time			25		nS
Q_g	Total Gate Charge (-10 V)	V_{DS} = -160 V V_{GS} = -10 V I_D = -5 A		25		nC
Q_{gs}	Gate-Source Charge			6		nC
Q_{gd}	Gate-Drain Charge			15		nC

Source-Drain Diode Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_S	Continuous Source Current [1,5]	V_G=V_D=0V, Force Current			-12	A
V_{SD}	Diode Forward Voltage [2]	I_S = -5 A , V_{GS}=0V , T_J=25℃			-1.3	V
t_{rr}	Reverse Recovery Time	I_F = -5 A , dI/dt = 100A/μs, T_J=25℃		17		nS
Q_{rr}	Reverse Recovery Charge			13		nC

Notes:

1.The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2.The data tested by pulsed : Pulse Width ≤ 300μs , Duty Cycle ≤ 2%.

3.The E_{AS} data shows Max. rating . The test condition is V_{DD} = -50 V , V_{GS} = -10 V , L = 0.5 mH , I_{AS} = -12 A.

4.The power dissipation is limited by 150℃ junction temperature.

5.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

Typical Characteristics

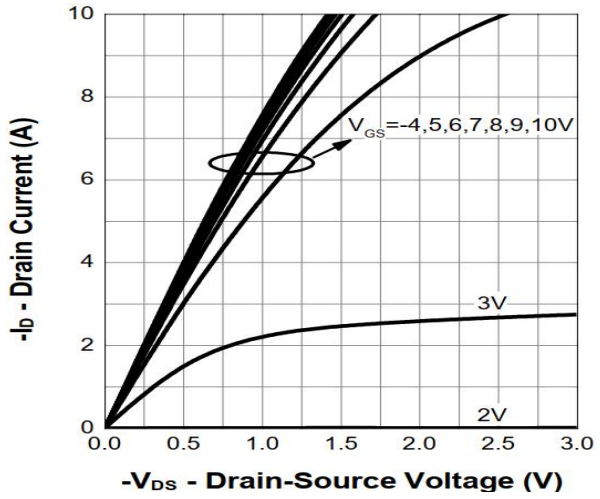


Fig.1 Typical Output Characteristics

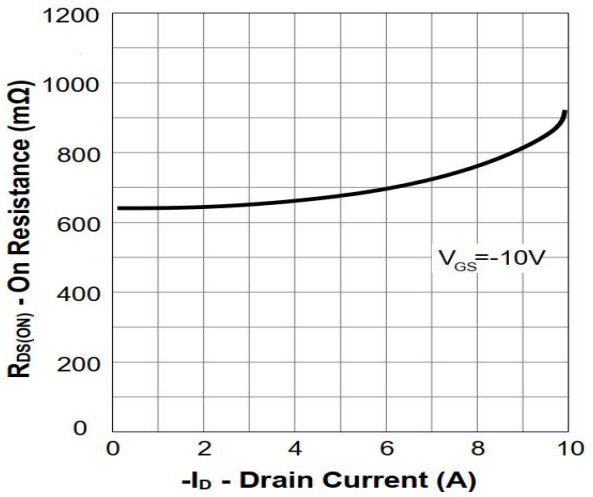


Fig.2 On-Resistance vs. Drain Current

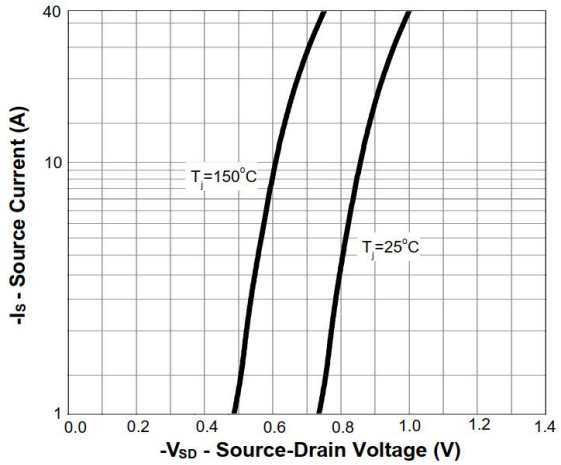


Fig.3 Forward Characteristics Of Reverse

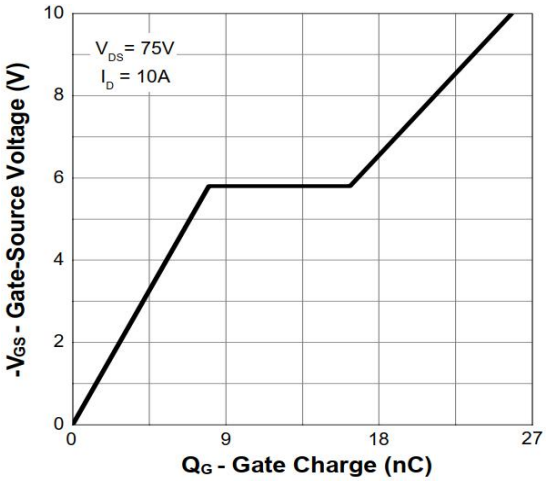


Fig.4 Gate-Charge Characteristics

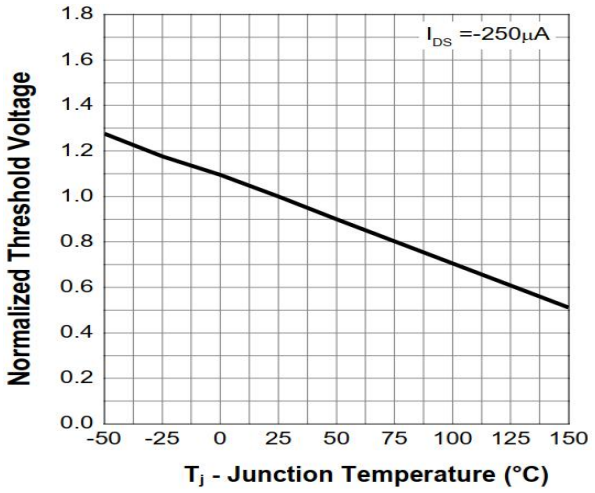


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

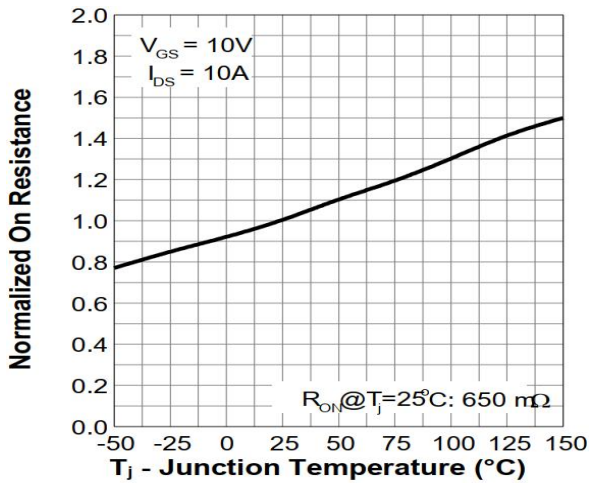


Fig.6 Normalized R_{DSON} vs. T_J

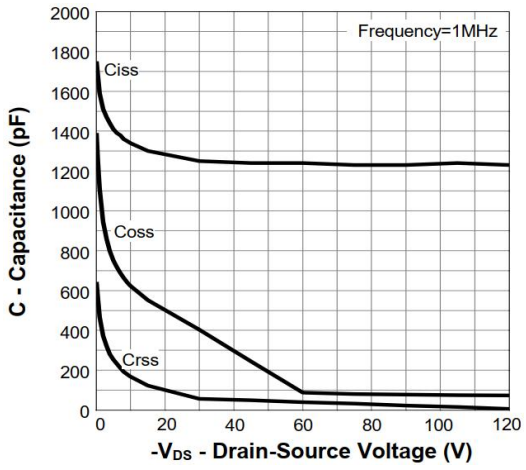


Fig.7 Capacitance

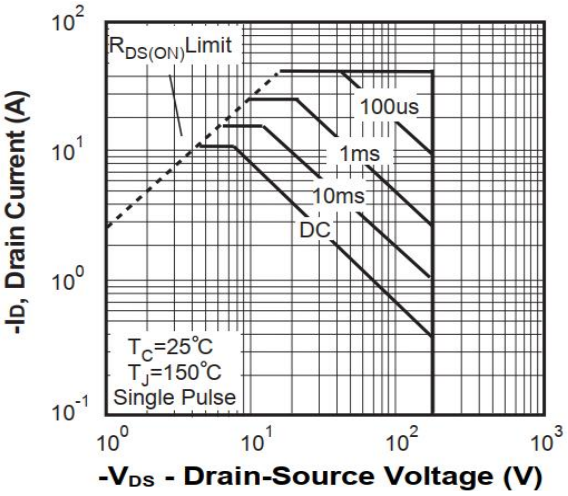


Fig.8 Safe Operating Area

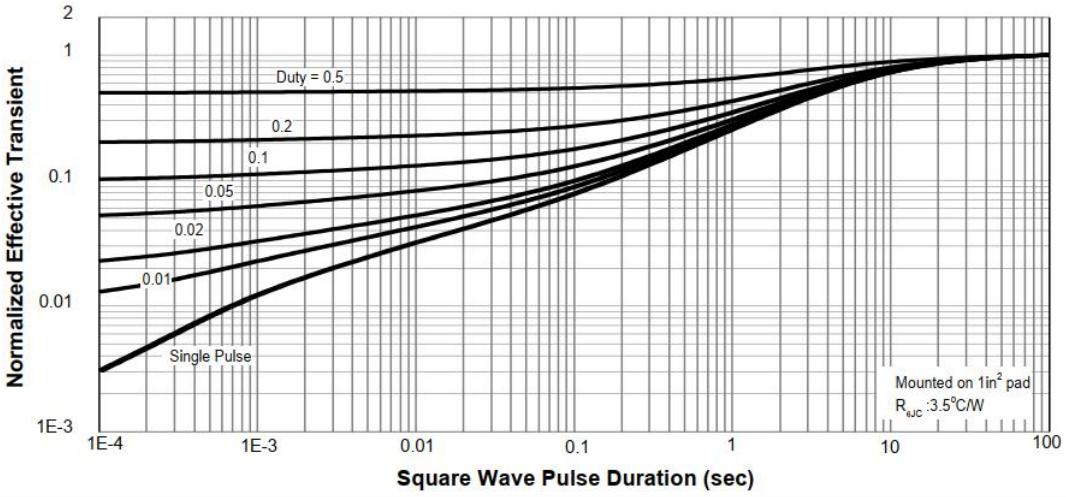


Fig.9 Normalized Maximum Transient Thermal Impedance

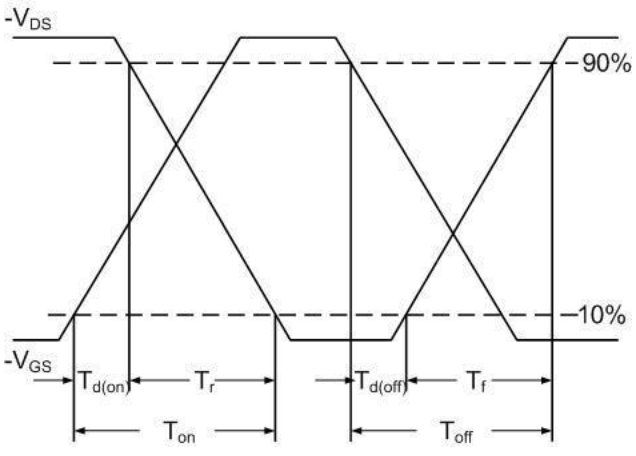


Fig.10 Switching Time Waveform

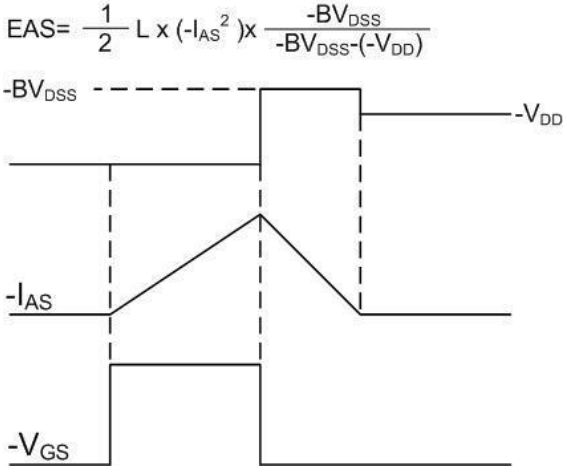
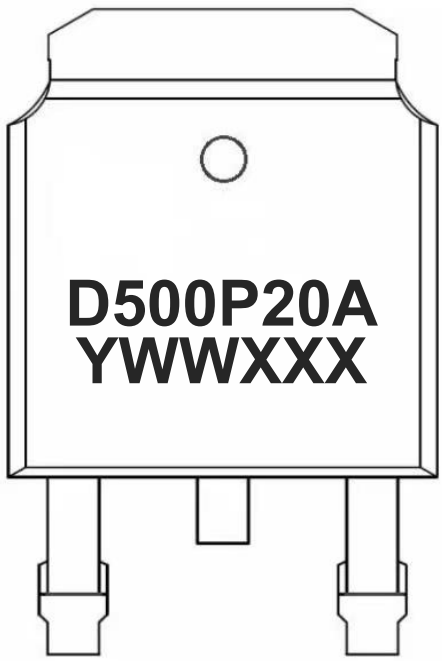


Fig.11 Unclamped Inductive Switching Waveform

Marking Information



1 st line： **HuaYuanWei Logo (left)**

2 nd line： **Device Package, Part Number, Channel and Version**

3 rd line： **Date Code [Y WW XX X]**

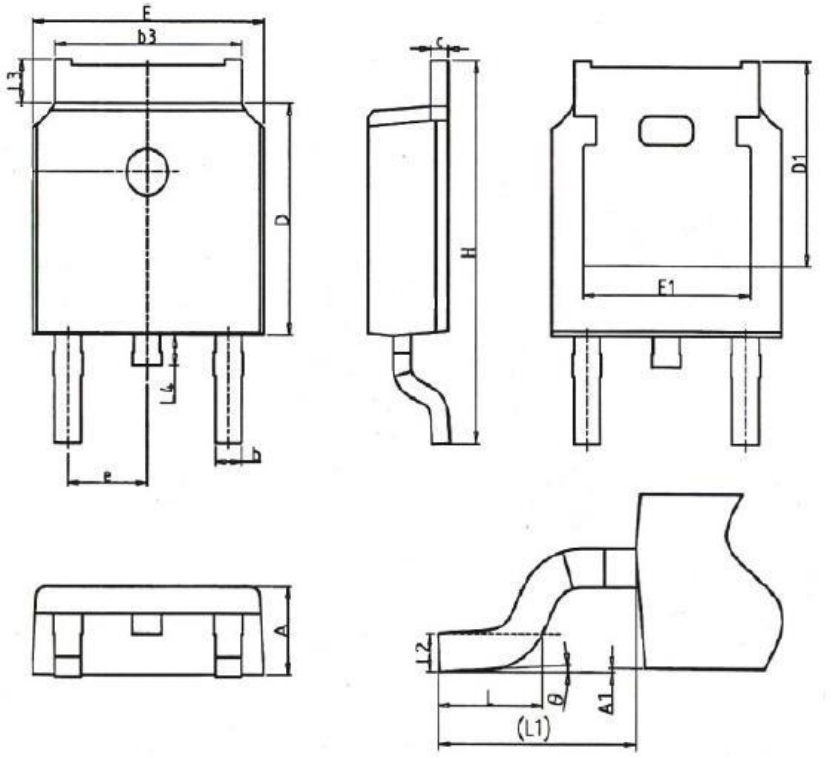
① **Y** **：** Year (2021=M, 2022=N……)

② **W W** **：** Week (01-53)

③ **X X** **：** Serial Number (01-99, AA-ZZ)

④ **X** **：** Factory Code (A-Z)

TO-252 Package Outline



SYMBOLS	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.18	2.40	0.086	0.095
A1	-	0.2	-	0.008
b	0.68	0.9	0.026	0.036
b3	4.95	5.46	0.194	0.215
c	0.43	0.89	0.017	0.035
D	5.97	6.22	0.235	0.245
D1	5.300REF		0.209REF	
E	6.35	6.73	0.250	0.265
E1	4.32	--	0.170	-
e	2.286BSC		0.09BSC	
H	9.4	10.5	0.370	0.413
L	1.38	1.78	0.054	0.070
L1	2.90REF		0.114REF	
L2	0.51BSC		0.020BSC	
L3	0.88	1.28	0.034	0.050
L4	0.5	1	0.019	0.039
Θ	0°	8°	0°	8°